PATENT

| | | | |
|---|---|---|---|
| Applicants: | Rajat Aggarwal et al. | | |
| Assignee: | Xilinx, Inc. | | |
| Title: | Method, System, and Apparatus for Incremental Design in Programmable Logic Devices Using Floorplanning | | |
| Serial No.: | 10/812,550 | File Date: | 03-29-04 |
| Examiner: | Paul Dinh | Art Unit: | 2825 |
| Docket No.: | X-1490 US | Conf. No.: | 3439 |

---

Mail Stop AMENDMENT
COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450

## INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Pursuant to 37 C.F.R. 1.56, Applicants bring to the attention of the Examiner the two (2) references listed in the attached Substitute for Form 1449A/PTO. A copy of each is enclosed herein.

The enclosed references are being cited after the receipt of a first office action but prior to any final action.

Citation of the above documents shall not be construed as an admission that the documents are necessarily prior art with respect to the instant invention. Citation of the above documents shall not be construed as a representation that a search has been made other than as described above. Also, the citation of the above documents shall not be construed as an admission that the information cited herein is, or is considered to be, material to patentability as defined in §1.56(b).

The Commissioner is hereby authorized to charge the fee of $180.00 due under 1.17(p) and any additional fees, or credit any overpayment which may be required to Deposit Account No. 24-0040.

Respectfully submitted,

06/08/2006 FKETEKI1 00000012 240040 10012550
01 FC:1806 180.00 DA

Kim Kanzaki, Ph.D.
Attorney for Applicants
Reg. No. 37,652

*I hereby certify that this correspondence is being deposited with the United States Postal Service as **first class mail** in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on June 5, 2006.*

Pat Tompkins — Pat Tompkins
*Name* *Signature*

PTO/SB/08A (10-01)
Approved for use through 10/31/2002. OMB 0651-0031
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE



Substitute for form 1449A/PTO

# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

| Complete if Known | |
|---|---|
| Application / Conf. No. | 10/812,550 / 3439 |
| Filing Date | March 29, 2004 |
| First Named Inventor | Rajat Aggarwal |
| Art Unit | 2825 |
| Examiner Name | Paul Dinh |
| Attorney Docket Number | X-1490 US |

## OTHER -- NON PATENT LITERATURE DOCUMENTS

| Examiner Initials * | Cite No.[1] | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | T[2] |
|---|---|---|---|
| | | Hiroshi Murata et al.; "VLSI Module Placement Based on Rectangle-Packing by the Sequence-Pair"; IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems; Vol. 15, No. 12; December 1996; Copyright 1996 IEEE; pp. 1518-1524. | |
| | | S. Kirkpatrick et al.; "Optimization by Simulated Annealing"; Science; Vol. 220, No. 4598; May 12, 1983; pp. 671-680. | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |

| Examiner Signature | | Date Considered | |
|---|---|---|---|

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number. [2] Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.